REMARKS

Claims 1 to 3 and 10 to 13 were pending in the present application. Claims 1 to 3 and 10 to 13 remain pending.

Claim Objection

Applicant has not amended claim 1 as suggested by the Examiner since claim 1 is correct. The third limitation of claim 1 recites "a memory copy write command for mirroring a write to a local node to a remote nodes by writing an entire line of memory from the local node to a line of memory at the remote node via one of the communication links when a new data is written into the line of memory at the local node even when the new data is smaller than the line of memory at the local node …." As recited, when a new data that is smaller than a line of memory is written to that line of memory, mirroring is performed to copy the entire line of memory to a remote node instead of just copying the new data to the remote node.

Double Patenting

Applicant has submitted herewith a terminal disclaimer in regards to U.S. Patent No. 6,973,484.

Rejections of Claims 1 to 3 and 10 to 12

The Examiner rejected claims 1 to 3 and 10 to 12 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,049,889 ("Steely, Jr. et al.") in view of U.S. Patent No. 5,850,556 ("Grivna"), further in view of U.S. Patent No. 4,520,439 ("Liepa"). The Examiner rejected claim 11 under 35 U.S.C. § 103(a) as being unpatentable over Steely, Jr. et al. in view of Grivna, further in view of U.S. Patent No. 5,914,970 ("Gunsualus et al.").

Claim 1

Addressing Applicant's first argument that Steely, Jr. et al. does not disclose a direct memory access (DMA) command, the Examiner stated:

> Steely further teaches a Memory Channel network and PCI Memory Channel adapters in col. 3, lines 22-29. Gillett in an analogous art teaches on page 246, right column, that a memory channel adapter connected to a PCI bus appears as a very high-speed DMA device for message received from the network. Therefore,

> an inter-node DMA transfer is being performed as far as the remote node is concerned);

July 24, 2006 Office Action, p. 4. Applicant respectfully traverses.

Steely, Jr. et al. does not disclose an inter-node DMA transfer from a local node to a remote node. As described in the November 3, 2005 Response to the September 12, 2005 Office Action, Steely, Jr. et al. discloses a local DMA operation that transfers data received at a local memory channel (MC) adaptor to a local system memory or a local I/O device at the completion of a reflected write. This is supported by a Rule 132 Declaration submitted along with the November 3, 2005 Response.

The Examiner cited an article by Gillett et al. entitled "Overview of Memory Channel Network for PCI" to support his argument that Steely, Jr. et al. discloses a DMA command from a local node to a remote node. Specifically, the Examiner cited the right column on p. 246 of Gillett et al., which states:

> A very high-speed DMA device for messages received from the network. These messages are mapped to host memory by the standard DMA maps used by all other PCI I/O devices.

Gillett et al., p. 246. The above quoted lines of Gillett et al. disclose that for receiving data from the network, the MC adapter acts as a DMA device that maps the data to a host memory. The above quoted lines of Gillett et al. do not disclose that the MC adapter performs an inter-node DMA transfer from a local node to a remote node. Instead, it confirms that after receiving data from a reflected write, the MC adapter performs a DMA transfer from its memory to a local system memory or a local I/O device.

Addressing Applicant's second argument that Steely, Jr. et al. does not disclose a memory copy write command that copies an entire line of memory from a local node to a remote node even when the line is only partially written with new data, the Examiner stated:

> Not explicitly disclosed by Steely is writing an entire line of memory from a local node to a remote node via one of the communication links even when the new data is smaller than the line of memory. However, Liepa in an analogous art teaches a method for partially writing data to a memory ranging from one bit to the length of word (col. 2, lines 47-50) wherein the new data (col. 7, line 67 to col. 8, line 2; Fig. 2, element 76) is merged with existing data (col. 8, lines 14-17); Fig. 2, elements 82 and 84 are masked existing data), and the entire memory word consisting of the merged data is written (Fig. 2, element 56).

Applicant agrees that Liepa discloses a partial write to a memory word where existing data is merged with new data. However, neither Liepa nor the other cited references disclose that after such a partial write, the entire memory word is copied from a local node to a remote node instead of copying only the new data from the local node to the remote node.

For the above reasons, amended claim 1 is patentable over the combination of Steely Jr. et al., Grivna, and Liepa for the above reasons.

Claims 2, 3, 10 to 12

Claims 2, 3, and 10 to 12 depend from amended claim 1 and are patentable over the cited references for at least the same reasons as amended claim 1.

Claim 13

The Examiner did not substantively reject claim 13. Accordingly, claim 13 is allowable subject matter after the submission of the terminal disclaimer.

Summary

In summary, claims 1 to 3 and 10 to 13 were pending in the present application. Applicant requests the Examiner to withdraw his claim objection/rejections and allow claims 1 to 3 and 10 to 13. Should the Examiner have any questions, please call the undersigned at (408) 382-0480x206.

Respectfully submitted,

/David C Hsia/

David C. Hsia
Attorney for Applicant(s)
Reg. No. 46,235

Patent Law Group LLP
2635 North First St., Ste. 223
San Jose, California 95134
408-382-0480x206